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HP E2449B

PowerPC Inverse Assemblers

The Hewlett-Packard Company E2449B inverse assembler supports several versions of the Motorola and IBM PowerPC families. The software configures the logic analyzer, labeling address, data, and status lines. Additionally, when a state trace is displayed the data is disassembled and listed in the appropriate PowerPC mnemonics.

Standard Features

Microprocessor Compatibility

The Motorola/IBM PowerPC 601 and 603 are supported. The IBM 403GA is also supported.

Microprocessor Speed

Maximum state analysis speeds are determined by the logic analyzer used. The HP 16550A is rated at 100 MHz, the HP 16554A at 70 MHz, the HP 16555A at 110 MHz, the HP 16556A at 100 MHz, and the HP 1660-series at 100 MHz. No hardware is supplied with this product.

Data Sampling Modes

• State-per-address or data cycle

In this mode, the logic analyzer records only those states in which one or more of the strobes are asserted. These strobes include AACK, ARTRY, TA, DRTRY, TEA for the PowerPC 601/603; IOTV (TS6) for the IBM PowerPC 403GA. This mode filters wait states, and exposes the PowerPC's decoupled address and data buses.

• State-per-clock mode

When using this mode, address and data are captured on each CPU clock. This feature is useful in hardware validation and debugging of system crashes.

For use with HP logic analyzers

• Timing mode

All address, data, and status lines are labeled on the logic analyzer display when making accurate timing measurements.

Inverse Assembler Features

All processor instructions are supported. In addition, disassembly is synchronized at branch addresses.

Logic Analyzers Supported

PowerPC 601/603

- HP 16550A (one required)
- HP 16554A (two required)
- HP 16555A (two required)
- HP 16556A (two required)
- HP 1660A (one required)

PowerPC 403GA

- HP 16550A (one required)
- HP 16554A (two required)
- HP 16555A (two required)
- HP 16556A (two required)
- HP 1661A (one required)
- HP 1660A (one required)

- **Number of probes required**

PowerPC 601/603: Eight, sixteen-channel probes are required for complete state disassembly. An additional two probes will monitor the remainder of the signal pins for timing measurements.

PowerPC 403GA: Five, sixteen-channel probes are required for complete state disassembly. An additional three probes will monitor the remainder of the signal pins for timing measurements.

- **Target signal timing**

Data must be valid for a 3.5 ns window with respect to the logic analyzer clock, which strobes bits into the logic analyzer on the rising edge. For the PowerPC 601, if BCLK_EN is used to pace the bus at a fraction of the microprocessor clock, then BCLK_EN=0 should be ANDed with the storage qualification term. This process is discussed in detail in the User's Guide.

- **Termination required**

You are responsible for providing a connection and termination scheme for the logic analyzer probes.

Several techniques are discussed in the application note, *Minimizing Intrusion Effects When Probing With A Logic Analyzer*, publication number 5962-8620E, available from the nearest HP Sales Office.

- **Evaluation board compatibility**

The IBM Microelectronics' PowerPC 403GA Evaluation Board, which includes 20-pin termination headers for an HP logic analyzer, is supported by the 403GA configuration file of the HP E2449B.

For more information, call your local HP sales office listed in your telephone directory, or an HP regional office listed below:

United States:

Hewlett-Packard Company
Test and Measurement Organization
5301 Stevens Creek Blvd.
Bldg. 51L-SC
Santa Clara, CA 95052-8059
1 800 452 4844

Canada:

Hewlett-Packard Canada Ltd.
5150 Spectrum Way
Mississauga, Ontario L4W 5G1
(905) 206-4725

Europe:

Hewlett-Packard
European Marketing Centre
P.O. Box 999
1180 AZ Amstelveen
The Netherlands
31 20 547 9858

Japan:

Yokogawa-Hewlett-Packard Ltd.
Measurement Assistance Center
9-1, Takakura-Cho, Hachioji-Shi,
Tokyo 192, Japan
(81) 426 48 3860

Latin America:

Hewlett-Packard
Latin American Region Headquarters
5200 Blue Lagoon Drive, 9th Floor
Miami, Florida 33126, U.S.A.
(305) 267 4245/4220

Australia/New Zealand:

Hewlett-Packard Australia Ltd.
31-41 Joseph Street
Blackburn, Victoria 3130
Australia
131 347 ext. 2902

Asia Pacific:

Hewlett-Packard Asia Pacific Ltd.
17-21/F Shell Tower, Time Square
1 Matheson Street, Causeway Bay
Hong Kong
(852) 2599 7070

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